Dr. Pallab Dasgupta

A K Singh Distinguished Chair Professor in Artificial Intelligence,
Department of Computer Science & Engineering,
Indian Institute of Technology Kharagpur.

Ph: +91-3222-282037 (Off),
+91-3222-283471 / 278710 (Res)
Fax: +91-3222-278985
Cell: +91-9434016141
Email: pallab@cse.iitkgp.ernet.in
Home: http://cse.iitkgp.ac.in/~pallab

Date of Birth: Oct 31, 1967
Nationality: INDIAN

EDUCATION

- Bachelor of Technology in Computer Science and Engineering from I.I.T. Kharagpur [1986-1990]. Ranked first in the department with a CGPA of 9.98 / 10.00.
- Master of Technology in Computer Science and Engineering from I.I.T. Kharagpur [1990-1992]. Ranked first in the department with a CGPA of 9.60 / 10.00.
- Ph.D in Computer Science and Engineering from I.I.T. Kharagpur [1992-1995].

AWARDS AND RECOGNITION

- Fellow of the Indian Academy of Science (since 2015)
- Fellow of the Indian National Academy of Engineering (since 2012)
- Fellow of the Institution of Electronics and Telecom Engineers, India (since 2013)
- A K Singh Distinguished Chair Professor in Artificial Intelligence, I.I.T. Kharagpur (2018 - 2020)
- Young Scientist Medal of Indian National Science Academy (1999)
- Young Engineer Medal of Indian National Academy of Engineering (2002)
- Associate of the Indian Academy of Sciences (1998 – 2002)
- IESA Technomentor Award (2012) conferred by the Indian Electronics and Semiconductor Association *for outstanding contributions in the field of Semiconductors / Electronics.*
- IBM Faculty Award (2007)
- Institute Silver Medal for 1st rank in BTech, Computer Sc & Engineering, IIT Kharagpur (1990)
- Institute Silver Medal for 1st rank in MTech, Computer Sc & Engineering, IIT Kharagpur (1992)
- Jagadis Bose National Science Talent Search Scholarship (1986 – 1990)

Pallab Dasgupta was named as one of *top 10 contributors in Computer Science in India in terms of number of publications during 2002 to 2014* in the DST bibliometric study: *International Comparative Performance of India's Research Base (2009-14) – A bibliometric analysis.* The study was commissioned by the Dept. of Science and Technology, Govt. of India. (Available online at: http://nstmis-dst.org/PDF/Elsevier.pdf and at https://www.elsevier.com/research-intelligence/research-initiatives/india-research-performance)

EMPLOYMENT

Position held	Institution	From	To
ACADEMIC POSITIONS			
Visiting Lecturer (Tenure track)	I.I.T. Kharagpur	Dec 1995	Feb 1998
Assistant Professor, Computer Sc & Engg	I.I.T. Kharagpur	Mar 1998	Jun 2002
Associate Professor, Computer Sc & Engg	I.I.T. Kharagpur	Jul 2002	Mar 2007
Professor, Computer Sc & Engg	I.I.T. Kharagpur	Apr 2007	Aug 2013
HAG Professor, Computer Sc & Engg	I.I.T. Kharagpur	Aug 2013	---
ADMINISTRATIVE POSITIONS			
Professor-In-Charge, Advanced VLSI Design Lab	I.I.T. Kharagpur	Oct 2007	Sep 2010
Associate Dean (Sponsored Res. & Industrial Consultancy)	I.I.T. Kharagpur	Oct 2013	Jul 2016
Dean (Sponsored Research & Industrial Consultancy)	I.I.T. Kharagpur	Aug 2016	---

PROFESSIONAL AND LEADERSHIP SERVICES

- Associate Editor, IEEE Trans. on Computer Aided Design of Integrated Circuits and Systems (2015-2018)
- Vice Chair (India) of IEEE Council on Electronic Design Automation (2016-2018)
- Council Member of Indian Association for Research in Computer Science (2013-2014)
- Founder and Joint Director of Synopsys CAD Laboratory, IIT Kharagpur along with Dr Pradip Dutta, President, Synopsys India Pvt. Ltd. (2009 -). This is the only academic research lab of Synopsys in Asia.
- Chairman, Advanced VLSI Consortium (consortium of 15 semiconductor and EDA companies) 2007-2010. This was the largest research consortium of semiconductor companies in the country at a time when the VLSI industry in India was growing in research.
- Founder of the Indo-German Center for Intelligent Transportation System in collaboration with Technical University of Munich, Germany. This is a very recent initiative.
- Founder and Principal Investigator of FMSAFE: Center for Formal Methods in Safety Critical Systems in partnership with IIT Bombay and IIT Kanpur. This center has been created under the IMPRINT programme.
- Co-Founder and Co-Principal Investigator of Center for Artificial Intelligence for Societal Needs, IIT Kharagpur
- Co-Founder and Co-Principal Investigator of Science and Heritage Initiative (SandHI), IIT Kharagpur
- Co-Founder and Co-Principal Investigator of General Motors Collaborative Research Lab, IIT Kharagpur
- Professor-in-charge of SPIC MACAY, IIT Kharagpur Chapter (2000 – 2016)
- Co-Founder of Advanced Manufacturing Consortium, IIT Kharagpur (conceived the consortium model as the Dean, Sponsored Research and Industrial Consultancy, IIT Kharagpur).

Professor Dasgupta plays an Indian Classical stringed instrument called the sitar. He is currently collaborating with Padmashree Pt Ajoy Chakraborty, renowned classical vocalist and scholar, who is a distinguished visiting professor of IIT Kharagpur. Together they are studying the deep structure of Indian Ragas and their representation as semi-lexical languages – a study which is expected to highlight the creative liberty in Indian Classical Music from a cognitive perspective. Professor Dasgupta is also spearheading an initiative for setting up an Academy of Classical Arts at IIT Kharagpur.

SPONSORED RESEARCH

- **Selected Industry Projects**

Domain: Verification of Digital Integrated VLSI Circuits	
1	Intel (Folsom, USA and Haifa, Israel) 2002 - 2005 (~150,000 USD) Formal methods for verification of architectural properties and computing formal coverage metrics was integrated into Intel's Formal Verification tool suite developed at Intel, Haifa.
2	National Semiconductor Corp., (Santa Clara, USA) 2003 – 2007 (~150,000 USD) A tool called GENSTIMULI was developed for the Technology Infrastructure Group of National Semiconductors (now TI), which uses formal methods for generating tests for custom cell characterization.
3	Synopsys (Bangalore, India and Massachusetts, USA) 2000 – 2008 (~30,000 USD) Design of Assertion Languages and Formal Specification Formalisms (some of which are now part of the SystemVerilog Standards). Several toolkits and patented verification technologies were developed.
4	Intel (Bangalore, India) 2009 – 2012 (~40,000 USD) Formal methods for post-silicon validation of bug-fixes and Counter-example Ranking in Intel's processors. The PhD student working in this project, Srobona Mitra, won the Google Anita Borg Woman in Engineering Award for this work.
5	Synopsys CAD Laboratory 2009 – Date (~4,00,000 USD) Synopsys CAD Labs, IIT Kharagpur was set up for undertaking projects in the areas of design automation for verification, testing, and security. Synopsys conferred the prestigious Charles Babbage Grant to this Lab.
Domain: Verification of Mixed-Signal Integrated Circuits	
1	National Semiconductor Corp., (Greenock, Scotland) 2007 – 2010 (~150,000 USD) Methods for verifying integrated power management units (PMUs) which are large integrated AMS circuits used in portable power devices like cell phones, PDAs and Laptops. The methods use formal hybrid automata based behavioral models.
2	Semiconductor Research Corporation (SRC), USA 2008 – Date (~200,000 USD) Technology for verification of formal analog properties over AMS simulators. Phase-2 of the project deals with abstract interpretation of formal equivalence features between AMS designs/models. SRC is a consortium of semiconductor and EDA companies.
3	Texas Instruments (custom funded through Semiconductor Research Corporation, USA) 2018 – 2021 (~150,000 USD) Technology for formal coverage management of large analog and mixed-signal integrated circuits.
Domain: Verification of Power Intent and Power Management Strategies	
1	Synopsys (California, USA and Bangalore, India) 2008 – 2013 (~60,000 USD) Formal verification technology for verifying the architectural power management strategy of large integrated circuits. A tool has been developed using the technology.
2	Intel (Bangalore, India) 2010 – 2012 (~60,000 USD) Tool for evaluating power management strategies for mobile portable platforms.

3	Intel Global Research (USA) 2015- Date (~240,000 USD) Formal verification of power management strategies for mixed-signal power domains.
Domain: Verification of Automotive Control	
1	General Motors (India Science Labs) 2007 – 2009 (~ 60,000 USD) Technology for verification of formal properties on the fly over execution traces of UML state-charts was integrated into a tool being used by GM for verification of automotive control software.
2	General Motors (India and Warren, USA) 2009 – 2012 (~ 60,000 USD) Formal verification of feature specifications for automotive control subsystems using AI planning techniques. This research led to a joint patent with General Motors.
Domain: Software Verification	
1	Google Inc. 2008 – 2009 (~ 50,000 USD) This was a one-time research grant from Google for developing formal methods for verifying web-service protocols
2	Hindustan Aeronautics Ltd. 2015 – 2018 (~ 50,77,000 INR) Formal verification of India's first indigenous avionic Real Time Operating System. The RTOS is now flying with the Hawkeye aircraft of HAL.
Domain: Verification of Railway Signaling and Interlocking	
1	Indian Railways 2013 -- 2017 Formal methods for proving the correctness of Electronic Interlocking Logic for railway signaling.

- **Selected Government Funded Projects**

1	**Artificial Intelligence For Societal Needs** (2013-2017) (5 Crores INR) This project funded under the Diamond Jubilee Research Grant, IIT Kharagpur brought together researchers from various departments to work for AI solutions to problems in Agriculture, Environment, Power, Disaster Management and Urban Planning. PIs: Pallab Dasgupta and Sudeshna Sarkar
2	**FMSAFE: A Networked Centre for Formal Methods for Safety Critical Systems** (2017-2020) (3.47 Crores INR) This IMPRINT project funded by MHRD and Ministry of Railways, brings together experts from IIT Kharagpur, IIT Bombay and IIT Kanpur to develop formal verification technology for safety critical systems. PI: Pallab Dasgupta CoPIs: Supratik Chakraborty, IIT Bombay, and Sandeep Shukla, IIT Kanpur
3	**Decoding And Exploring Ancient Classification of Ragas In Indian Classical Music (**2014-2018) (1.5 Crores INR) This project was funded by MHRD under the Science and Heritage Initiative (SandHI). Pallab Dasgupta is collaborating with Indian Classical musicians in studying the deep structure of Indian Ragas. PIs: Pallab Dasgupta and Priyadarshi Patnaik.
4	**AUTOSAFE: Architecture- Aware Timing Analysis And Formal Verification of Automotive Control Systems** (2012-2015) (2.91 Crores INR) This project was funded by the Indo-German Science and Technology Center to IIT Kharagpur and TU Munich. This project laid the foundations for the two universities to come together to set up an Indo-German Center for Intelligent Transportation Systems at IIT Kharagpur recently.

TOOLS AND TECHNOLOGY

PATENTS

US PATENT No: US 7,797,123 Sep 14, 2010

- ***Method and Apparatus for Extracting Assume Properties from a Constrained Random Test Bench***, Inventors: K.Dey, E.Cerny, Pallab Dasgupta, B.Pal, P.P.Chakrabarti.

  This patent describes a technique for automatically extracting formal logical constraints on the environment of a circuit, where the environment is described by means of a test-bench developed in SystemVerilog. Developing environment constraints (called *assume properties*) is a non-trivial task and is one of the main concerns in formal verification of reactive systems. The patented technique automated this problem. The patent was jointly obtained with collaborators from Synopsys Inc, and is assigned to Synopsys.

US PATENT No: US 8,082,140, Dec 20, 2011

- ***Parametric Analysis of Real Time Response Guarantees on Interacting Software Components***, Inventors: M.Dixit, S.Ramesh, Pallab Dasgupta.

  This patent describes a technique for automatic extraction of linear constraints on the timing of constraint behaviors that are obtained by formally comparing the conjunction of component specifications with formal time-critical end-to-end behaviors in automotive features. The patented technique enables early timing analysis with the help of formal specifications in the development of automotive control features and sub-system technical specifications. The patent was jointly obtained with collaborators from General Motors, and is assigned to General Motors.

TOOLS DEVELOPED BY THE RESEARCH GROUP

COV-ANALYZER

Formal verification coverage analysis tool. This tool has been integrated with the Forspec/Forecast tool suite of Intel with collaboration with the electronic design automation group at Intel, Haifa. The development of this tool was sponsored by the chipset design group at Intel, Folsom, USA.

SPEC-MATCHER

Formal design intent verification tool for digital integrated circuits. This tool was also developed under the research collaboration with Intel. These contributions have been noted in the article, *Fifteen Years of Formal Property Verification at Intel* by Dr Limor Fix, Director, Intel Research Lab, Pittsburgh, in the book, *25 Years of Model Checking*, Springer, 2008, ISBN: 978-3-540-69849-4.

CHASSIS

Verification tool for integrated power management chips. This tool was developed under a collaboration with National Semiconductor Corp, UK for verifying integrated PMUs, which are large scale analog-mixed circuits consisting of linear drop-out regulators, buck regulators and battery chargers. The tool introduced

the use of behavioral models based on hybrid automata into the design validation flow of National semiconductors.

POWER-TRUCTOR

Formal verification tool for verifying the architectural power management strategy in large digital integrated circuits. This tool has been developed recently under the Synopsys CAD Laboratory at IIT Kharagpur, and has been been reported in a recent paper in IEEE Trans. of VLSI.

CHAMS, DYFET AND FORFET: AMS ASSERTION AND FEATURE EVALUATION TOOLS

This tool suite enables any standard AMS circuit simulator to monitor analog time domain properties and features. These were developed under a recent project sponsored by the Semiconductor Research Corporation (SRC) which is a consortium of semiconductor and EDA companies. One version of this tool has been adopted by Freescale Semiconductors (now NXP).

GEN-STIMULI

This tool was developed for generating minimum length stimulus patterns for custom cell characterization. Adopted by National Semiconductors, this tool uses formal state space analysis to find the shortest stimuli for characterization tests like setup and hold.

RAILTOOLS FOR SIGNALING VALIDATION

This tool suite proves the correctness of signaling logic developed for electronic signaling and interlocking systems using formal methods. The tool has been tested on several railway yards in India and is now being considered by RDSO for widespread adoption in the Indian Railways.

PHD THESIS GUIDANCE

1. Design Intent Verification by Formal Property Coverage, ***Prasenjit Basu.*** [Currently working for AMD, Bangalore]

2. Formal Analysis of Property Specifications: Consistency, Coverage and Synthesis, ***Sayantan Das*** [Currently working for Verific Design Automation Pvt Ltd]

3. Formal Methods for accelerating formal, semi-formal and dynamic property verification through novel specification styles, ***Ansuman Banerjee*** [Currently holding Faculty Position at the Indian Statistical Institute (ISI) Kolkata]

4. SAT Based Solutions for Timing and Power Estimation in Gate Level Circuits, ***Suchismita Roy*** [Currently holding Faculty Position at NIT Durgapur]

5. Formal and semi-formal verification methods with constrained random test benches, ***Bhaskar Pal*** [Currently working for Synopsys in Formal Verification]

6. A symbolic event propagation approach for solving timing problems of digital circuits, ***Arijit Mondal*** [Currently holding Faculty Position at IIT Patna]

7. Model checking techniques for Reasoning about Events and Extremal Properties in Timed Systems, ***Jatindra Kumar Deka*** [Currently holding Faculty Position at IIT Guwahati]

8. Formal Methods for Early Time-Budgeting in Component-based Embedded Control Systems, ***Manoj Dixit*** [Currently with Mathworks, Bangalore]

9. Formal Analysis of Security Policy Implementations in Enterprise Networks, ***Padmalochan Bera*** [Currently holding Faculty Position at IIT Bhubaneswar]

10. Assertions – from a mixed-signal perspective, ***Subhankar Mukherjee*** [Currently with Mentor Graphics, Bangalore]

11. Formal and Semi-Formal Methods for Application Specific Usage Control and Security, ***Rajkumar P.V.*** [Currently Post Doc fellow at the Institute for Cyber Security, Univ of Texas, San Antonio, USA]

12. Formal Methods for Aiding Verification of Local Design Changes in Digital Integrated Circuits, ***Srobona Mitra*** [Currently Formal Verification Engineer at Synopsys India, Bangalore]

13. Search Techniques for finding Alternative Solutions for AND/OR Graphs and Bi-objective Optimization Problems, ***Priyankar Ghosh*** [Currently works for Synopsys India, Bangalore]

14. Formal Methods for Architectural Power Intent Verification and Functional Reliability Analysis, ***Aritra Hazra*** [Currently holding faculty position at IIT Kharagpur]

15. Automated Planning Based Methods for Early Verification of Reactive Control Systems, ***Kamalesh Ghosh*** [Currently working in Synopsys India, Bangalore]

16. Assertion Based Analysis of Mixed Signal Systems, ***Antara Ain***

TEACHING

- **Core Subjects of Computer Science**

    1. Foundations on Computing Science
    2. Programming and Data Structures
    3. Algorithms
    4. Operating Systems
    5. Introduction to Computing

- **Electives**

    1. Artificial Intelligence
    2. Applied Graph Theory
    3. Database Management Systems
    4. Distributed Computing Systems
    5. Testing and Verification of Circuits
    6. Formal Systems

- **Courses taken in other departments**

    1. Operations Research (Industrial Engineering & Management)
    2. Intelligent Management Systems (School of Management)
    3. Graphical User Interface Design (Industrial Engineering & Management)
    4. Automated Algorithms for Operations Management (Industrial Engineering & Management)
    5. Embedded Software Design and Validation (Advanced Technology Development Center)

VIDEO COURSES

- Artificial Intelligence – *contributed to NPTEL in 2009 and highly accessed even today*
- Distributed Systems
- Verification
- GUI Design -- *one of the first distance education courses recorded in the country*

PEDAGOGY COURSE UNDER NMEICT TALK-TO-TEN-THOUSAND-TEACHERS SCHEME

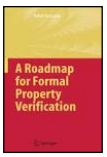
- **Algorithms – from a pedagogical perspective.**
  Jointly offered by Prof PP Chakrabarti and Prof PP Das to 10000 teachers through the National Knowledge Network.

INDUSTRY COURSE

- **Formal Verification Techniques for Digital Circuits.**
  Jointly offered by Prof P P Chakrabarti and Dr Ansuman Banerjee to 400 verification engineers at Texas Instruments.

PUBLICATIONS

BOOKS



A Roadmap for Formal Property Verification.
Pallab Dasgupta**,** Springer, 2006.

Multi-objective Heuristic Search.
Pallab Dasgupta**,** P.P. Chakrabarti, S.C. DeSarkar,
Vieweg Verlag, Germany, 1999.

Cohesive Coverage Management Leveraging Formal Test Plans
Artitra Hazra, Pallab Dasgupta, P.P. Chakrabarti, Lambert Academic Publishing, 2012

BOOK CHAPTERS

	Book Chapters	Authors	Publisher, Year
1	*Can Semi-Formal be made more Formal?* Book Title: *Next Generation Design and Verification Methodologies for Distributed Embedded Control Systems.* Ed: S.Ramesh, P.Sampath.	Ansuman Banerjee, Pallab Dasgupta, P.P. Chakrabarti	Springer, 2007
2	*Agent Searching.* Book Title: *Computational Mathematics, Modelling and Algorithms*	Pallab Dasgupta**,** P.P. Chakrabarti, S.C.DeSarkar	Narosa Publishing House, 1999
3	*Early Time Budgeting for Component-Based Embedded Control Systems.* Book Title: *Embedded Systems Development* Ed: A. S-Vincentelli, H. Zeng, M.Di-Natale, P.Marwedel	Manoj J Dixit, S. Ramesh, Pallab Dasgupta	Springer, 2014
4	*Formal Assurance of Signaling Safety: A Railways Perspective.* Book Title: *Handbook of Research on Emerging Innovations in Rail Transportation Engineering* Ed: B Umesh Rai	Pallab Dasgupta Mahesh Mangal	IGI Global, May 2016
5	*A Logical Perspective of Formal Verification: A Narrative on the Genesis and Evolution of the Formal Verification Group at IIT Kharagpur* Book Title: *The Mind of an Engineer* Ed: Purnendu Ghosh, Baldev Raj, INAE	Pallab Dasgupta	Springer 2016
6	*On the Deep Structure of Ragas and Analytic Rating of Music Scores* Book Title: *Heritage Preservation – A computational approach* Ed: Bhabatosh Chanda, Subhasis Chaudhuri, Santanu Chaudhury	Sudipa Mandal, Shilpi Chaudhuri, Antonio Anastasio Bruto da Costa, Gouri Karambelkar, Pallab Dasgupta	Springer 2018

JOURNAL PUBLICATIONS (BY AREA)

FORMAL MODELING AND LOGIC FORMALISMS

1. P.Dasgupta, Jatindra K. Deka and P.P.Chakrabarti. Model checking on Timed Event Structures. *IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems*, Vol 19, No 5, May 2000, 601-611.

2. P.Dasgupta, Jatindra K. Deka, P.P.Chakrabarti and S. Sriram. Min-max Computation Tree Logic. *Artificial Intelligence*, 127 (2001), 137-162.

3. P. Dasgupta, P.P.Chakrabarti, J.K. Deka. Min-max event triggered computation tree logic. *Sadhana, (Spl. Issue on Formal Verification),* 27 (2): 163-180, 2002.

4. A.C.Patthak, I.Bhattacharya, A.Dasgupta, P.Dasgupta, P.P.Chakrabarti. Quantified Computation Tree Logic. *Information Processing Letters,* 82(3): 123-129, 2002.

5. K. Chatterjee, P. Dasgupta, P.P. Chakrabarti. A branching time temporal framework for Quantitative Reasoning. *Journal of Automated Reasoning,* 30: 205-232, 2003.

6. K. Chatterjee, P. Dasgupta, P.P. Chakrabarti. The power of first-order quantification over states in branching and linear time temporal logics. *Information Processing Letters,* 91: 201-210, 2004.

7. A. Banerjee and P. Dasgupta. The Open Family of Temporal Logics: Annotating Temporal Operators with Input Constraints. *ACM Transactions on Design Automation and Embedded Systems (TODAES),* 10 (3), 492-522, 2005.

8. M. Dixit, S.Ramesh and P. Dasgupta. Some results on Parametric Temporal Logic. *Information Processing Letters,* 111(20): 994-998, 2011.

9. Subhankar Mukherjee, P. Dasgupta, A Fuzzy Real Time Temporal Logic*, Int. J. Approx. Reasoning*, 54(9): 1452-1470, 2013.

ADVANCED VERIFICATION METHODS FOR INTEGRATED CIRCUITS

10. P.Basu, S.Das, A.Banerjee, P. Dasgupta, P.P. Chakrabarti, C.R. Mohan, L.Fix, R.Armoni. Design Intent Coverage – A New Paradigm for Formal Property Verification. *IEEE Transactions on CAD,* 25 (10) 1922-1934, 2006.

11. B.Pal, A.Banerjee, P. Dasgupta, and P.P. Chakrabarti. BUSpec: A framework for generation of verification aids for Standard Bus Protocol Specifications. Integration – the VLSI Journal, Elsevier, Vol 40, I3, pp. 285-304, 2007.

12. Bhaskar Pal, Arnab Sinha, P. Dasgupta, P.P. Chakrabarti, Kaushik De, Hardware Accelerated Constrained Random Test Generation, IET Computers and Digital Techniques, vol. 1, no. 4, 423-433, 2007

13. Arnab Sinha, Pallab Dasgupta, Bhaskar Pal, Sayantan Das, Prasenjit Basu, P.P. Chakrabarti, Design Intent Coverage Revisited. *ACM Transactions on Design Automation of Electronic Systems*, 14 (1) 2009, 9:1—9:32.

14. Bhaskar Pal, Ansuman Banerjee, Arnab Sinha, Pallab Dasgupta, Accelerating Assertion Coverage with Adaptive Test-benches, IEEE Transactions on CAD (TCAD), Volume 27, Issue 5, Pages:967 - 972, May 2008.

15. Ansuman Banerjee, Pallab Dasgupta, P.P. Chakrabarti, Auxiliary state machines + context triggered properties in verification. *ACM Transactions on Design Automation of Electronic Systems*, 13 (4), 2008, 62:1—62:31.

16. S. Mitra, P. Ghosh and P. Dasgupta, Verification by parts: Reusing component invariant checking results, *IET Computers and Digital Techniques,* 6(1): 19-32, Jan 2012.

17. S. Das, A. Banerjee and P. Dasgupta, Early analysis of critical faults: An approach to test generation from formal specifications. *IEEE Transactions on CAD (TCAD)*, 31(3):447-451, March 2012.

18. Aritra Hazra, Priyankar Ghosh, Pallab Dasgupta and P. P. Chakrabarti, Cohesive Coverage Management: Simulation Meets Formal Methods, Journal of Electronic Testing: Theory and Applications (JETTA), vol. 28, no. 4, pp. 449-468, 2012.

19. Srobona Mitra, Ansuman Banerjee, Pallab Dasgupta, Priyankar Ghosh, Harish Kumar: Formal Guarantees for Localized Bug Fixes. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 32(8): 1274-1287, 2013

20. Srobona Mitra, Ansuman Banerjee, Pallab Dasgupta and Harish Kumar, Counterexample Ranking Using Mined Invariants, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Sytems, 32(12), 1978-1991, 2013.

FORMAL VERIFICATION OF TIMING AND POWER

21. Suchismita Roy, P. Dasgupta, P.P. Chakrabarti, Event propagation for accurate circuit delay calculating using SAT, *ACM Transactions on Design Automation of Electronic Systems,* 12(3), 2007, 36:1—36:23.

22. S.Roy, P.P.Chakrabarti, Pallab Dasgupta, Satisfiability Models for Maximum Transition Power, *IEEE Transactions on VLSI* Systems, 16 (8), 2008 941—951.

23. A.Mondal, P.P.Chakrabarti, P.Dasgupta, Statistical Timing Analysis using Symbolic Event Propagation, *IET Circuits, Devices & Systems*, 1(4), 2007, 283—291.

24. Suchismita Roy, P.P. Chakrabarti and P. Dasgupta. Bounded Delay Timing Analysis and Power Estimation using SAT, Microelectronics Journal, 41(5), May 2010, 317—324.

25. A.Mondal, P.P. Chakrabarti and P. Dasgupta. Symbolic event propagation based minimal test set generation for robust path delay faults, *ACM Transactions on Design Automation of Electronic Systems,* vol. 17 (4), 2012.

26. S. Roy, P.P. Chakrabarti and P. Dasgupta, SAT based timing analysis for fixed and rise/fall gate delay models, *Integration VLSI J*, Elsevier, 40(4), 357-364, 2012.

27. P. Ghosh, A. Hazra, R. Gonnabhaktula, N. Bhilegaonkar, P. Dasgupta, C.R. Mandal and K. Paul. Power-SIM: An SOC simulator for estimating power profiles of mobile workloads, *Journal of Low Power Electronics,* vol. 8, no. 3, pp. 293-303, 2012.

28. Aritra Hazra, Sahil Goyal, Pallab Dasgupta and Ajit Pal, Formal Verification of Architectural Power Intent, *IEEE Transaction on VLSI Systems (TVLSI),* vol. 21, no. 3, pp. 78-91, 2013.

29. Rajdeep Mukherjee, Priyankar Ghosh, Pallab Dasgupta and Ajit Pal, A Multi-Objective Perspective for Operator Scheduling using Fine-Grained DVS Architectures, International journal of VLSI design and Communication Systems (VLSICS), 4(1), 105-122, 2013.

30. Rajdeep Mukherjee, Priyankar Ghosh, Pallab Dasgupta and Ajit Pal, An Integrated Approach for Fine-Grained Power and Temperature Management During High-level Synthesis, Journal of Low Power Electronics (JOLPE), 9(3), 350-362, 2013.

31. Aritra Hazra, Rajdeep Mukherjee, Pallab Dasgupta, Ajit Pal, Kevin Harer, Ansuman Banerjee, Subhankar Mukherjee: POWER-TRUCTOR: An Integrated Tool Flow for Formal Verification and Coverage of Architectural Power Intent. IEEE Trans. on CAD of Integrated Circuits and Systems 32(11): 1801-1813, 2013.

32. Pallab Dasgupta, M.K. Srivas, Rajdeep Mukherjee, Formal Hardware/Software Co-Verification of Embedded Power Controllers, IEEE Transactions on CAD of Integrated Circuits and Systems, 33(12), 2025-2029, 2014.

ANALOG / MIXED-SIGNAL CAD FOR VERIFICATION

33. Rajdeep Mukhopadhyay, S K Panda, Pallab Dasgupta, John Gough, Instrumenting AMS Assertion Verification on Commercial Platforms *ACM Transactions on Design Automation of Electronic Systems*, 14 (2), 2009, 21:1—21:47

34. Rajdeep Mukhopadhyay, Anvesh Komuravelli, Pallab Dasgupta, Subrat K. Panda, Siddhartha Mukhopadhyay. A static verification approach for architectural integration of mixed-signal integrated circuits, Integration - the VLSI Journal, Elsevier Pub., 43(1), Jan 2010, 58—71.

35. Antara Ain, Debjit Pal, Pallab Dasgupta, S. Mukhopadhyay, R. Mukhopadhyay, John Gough. Chassis: A Platform for Verifying PMU Integration using Auto-Generated Behavioral Models, *ACM Transactions on Design Automation of Electronic Systems,* 16(3), June 2011.

36. Subhankar Mukherjee, P. Dasgupta, S. Mukhopadhyay. Auxiliary Specifications for Context-Sensitive Monitoring of AMS assertions, *IEEE Transactions on CAD (TCAD),* 30(10): 1446-1457, 2011.

37. Subhankar Mukherjee, Pallab Dasgupta, Siddhartha Mukhopadhyay, Scott Little, John Havlicek, Srikanth Chandrasekaran: Synchronizing AMS Assertions with AMS Simulation: From Theory to Practice. ACM Trans. Design Autom. Electr. Syst. 17(4): 38 (2012)

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